

General description

This data sheet describes a general purpose headphone amplifier (HPA) in a 140nm CMOS process.

The amplifier can drive loads down to 16Ω and with a supply voltage ranging from 1.5 Volt to 5 Volt.

With the internal feedback resistors the gain of the amplifier is +2 or -1 depending on which input is used.

Features

- Fixed gain of +2 or -1
- Supply voltage 1.5 to 5V
- Load impedance $\geq 16\Omega$
- $SNR_{@5mW}$ 101dB
- $THD_{@5mW,1kHz}$ 0.03%
- $0.125mm^2$ in $0.14\mu m$ CMOS

Applications

- Cellular Phones / Music Phones
- Smart Phones
- Portable Media / MP3 Players
- Portable CD / DVD Players

Block diagram

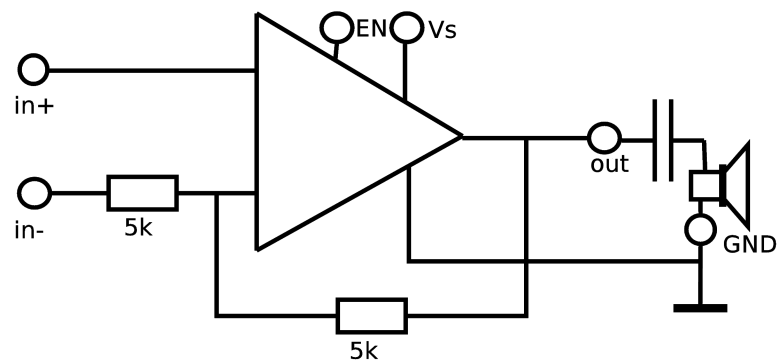


Figure 1: Block diagram headphone amplifier

Detailed description

The headphone amplifier (HPA) is a class AB amplifier in a standard 180nm CMOS process. The input requires a DC bias network to set the output voltage at half the supply voltage $V_{S+}/2$. This biasing network must be decoupled to ground for an optimal PSRR.

Applications with DC coupling ('true ground' application) are possible when a positive and a negative supply voltage are used ($\pm 0.75V$ to $\pm 2.5V$). It must be noticed that the substrate of the chip is connected to the negative supply pin. Combining the HPA with other circuits that are designed for a single supply voltage on the same chip is not possible when those circuits make use of the same 'signal' ground. Such a combination is possible when a P-well is added for the NMOS transistors as a process option.

Specifications

$V_{S+}=1.8V$, $R_{LOAD}=32\Omega$, $P_{OUT@1\%THD}$, $T=25^{\circ}C$ unless otherwise noted.

Parameter	Description	Min	Typ	Max	Units
Supply					
V_{S+}	Supply voltage	1.5	1.8	5	V
I_Q	Quiescent current		1		mA
Performance					
P_{OUT}	Output power		10		mW
$P_{OUT@16\Omega}$	Output power at 16Ω , $V_{S+}=1.8V$		19		mW
$P_{OUT@16\Omega, V_{S+}=3.3V}$	Output power at 16Ω , $V_{S+}=3.3V$		69		mW
THD	Distortion at $P_{OUT}=5\text{ mW}$, 1 kHz		0.03		%
SNR_{MAX}	Signal to Noise Ratio at $P_{OUT}=5\text{ mW}$, 1 kHz BW = 20kHz		101		dB
V_{NOISE}	Output noise, BW = 20kHz		2.5		μV
$PSRR_{@1kHz}$	Power Supply Rejection Ratio at 1kHz		51		dB
$PSRR_{@217Hz}$	Power Supply Rejection Ratio at 217Hz		51		dB
R_{LOAD}	Allowed load impedance	16			Ω
Implementation					
A_{C18}	Chip area in CMOS 140nm		0.125		mm ²

Table 1: Specifications

Typical Characteristics

Measured THD
inverting mode (gain=-1)

Supply = 3.3V, $R_{LOAD} = 32\Omega$, input = 1kHz sine, T = 25°C

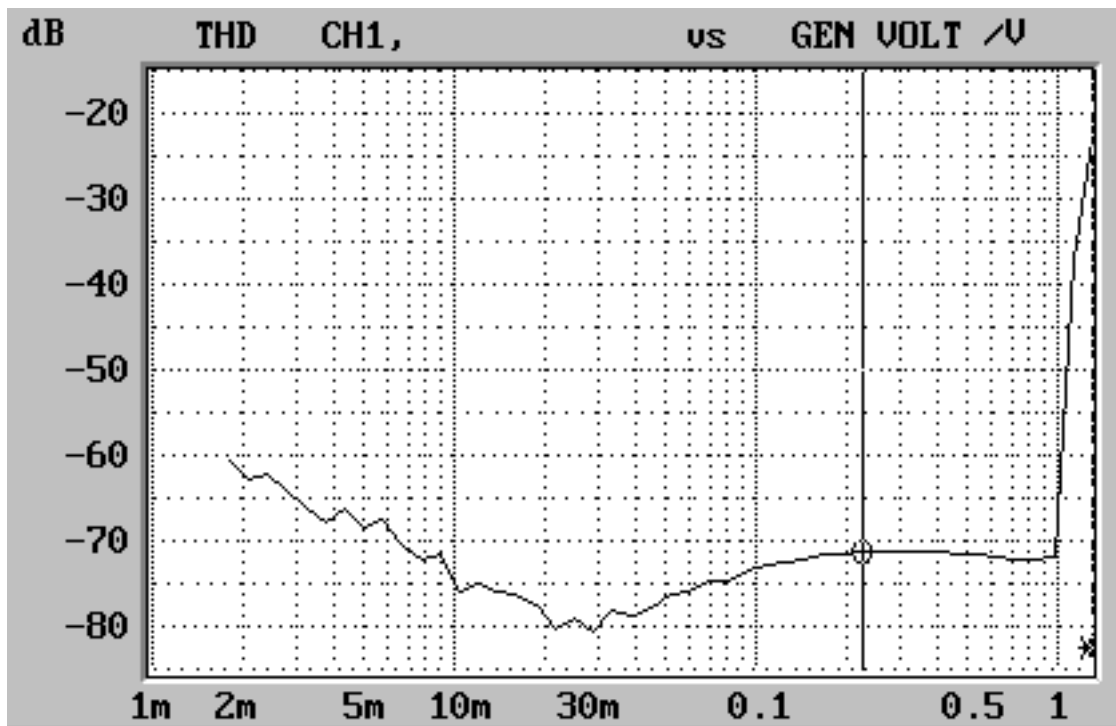


Figure 2: THD versus RMS output voltage

Port list

Port name	width	Description
<i>in+</i>	1	Non-inverting input
<i>in-</i>	1	Inverting input
<i>out</i>	1	Output
<i>EN</i>	1	Enable (active high)
<i>Vs</i>	1	Positive supply
<i>GND</i>	1	Ground

Table 2: Port function descriptions

Deliverables

The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement. A GDSII layout (version F1) is available for these purposes.

Revision history

Revision	Date:	Reason for revision
F1	2010-04-27	Initial version

Axiom IC is a design house that develops integrated circuits for silicon chips. Axiom IC focuses on the design of state-of-the-art analog and mixed signal circuits in CMOS and BiCMOS, in close cooperation with its customers. Based on our long history in industrial IC design and research, we are able to design robust IC's with short design cycles and high quality levels. Our goal is to use our expertise for customer specific design services, covering the entire range from feasibility studies and design to layout and verification.

A continuously growing IP portfolio enables us to quickly respond to customer demands giving you a short time to market. For more information please look at the web-site www.axiom-ic.com or send an e-mail to: info@axiom-ic.com

Axiom IC B.V.
Colosseum 28
7521 PT Enschede
The Netherlands

Phone: +31 (0)53-7370010
Fax: +31 (0)53-7370011
Email: info@axiom-ic.com
Web: www.axiom-ic.com