

General description

A PWM sigma-delta modulator is a special type of 1-bit sigma-delta modulator that produces a pulse width modulated (PWM) output signal with a fixed repetition frequency. A fixed repetition frequency makes the output signal insensitive to typical problems associated with (continuous time) sigma-delta converters, such as non-linear inter symbol interference (ISI) and kickback noise on the reference of the DAC.

This IP block implements a digital PWM sigma-delta modulator consisting of a fifth-order loop filter, followed by a 16 taps moving average filter, a sawtooth carrier injection (with a frequency of $f_{CLK}/16$) and a 1-bit quantizer. The functional block diagram is shown in Figure 1.

Features

- 117 dB dynamic range
- -120 dBFS inband noise
- ISI insensitive bit stream
- No signal dependent kick back on DAC reference
- Multi bit advantages with a single bit modulator
- Hardware costs ~ 700 gates
- 0.018 mm² in 0.14µm CMOS
- Silicon proven

Applications

- high accuracy PCM to PWM conversion
- signal generation for Class-D amplifiers
- D/A converters
- Audio subsystems
- Audio amplifiers with digital inputs
- Ideal in combination with FIRDAC (114dB DR measured)
- FPGA solution with discrete DAC (110dB DR measured)

Block diagram

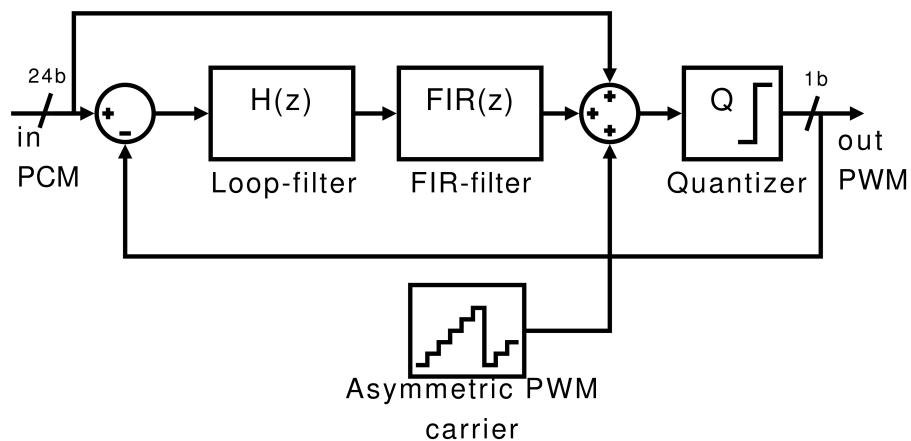


Figure 1: Block diagram PWM modulator

Proven performance

The PWM $\Sigma\Delta$ modulator was introduced in literature by [Doorn2005]. In that paper, results of a D/A converter show that the PWM $\Sigma\Delta$ modulator enables high audio performance (106dB SNDR_{max}, 114dB dynamic range, A-weighted) with very simple 1-bit DAC components. That paper also shows that the PWM $\Sigma\Delta$ modulator is very suitable to operate together with a FIRDAC (also known as a 'semi-digital reconstruction filter').

In another experiment, with the PWM $\Sigma\Delta$ modulator implemented on an FPGA and a DAC build from common off the shelf (COTS) components (a 74HCT574, 8 resistors, an Op-amp and an RC feedback network), an audio performance of 110dB dynamic range and 97dB SNDR_{max} was measured.

Detailed description

A functional block diagram of the PWM $\Sigma\Delta$ modulator is shown in Figure 1. It differs from a standard $\Sigma\Delta$ modulator in two ways:

- A digital 16 step sawtooth is added to the output signal of the loop filter to force a PWM output signal with a fixed switching frequency of $f_{CLK}/16$.
- The loop filter is cascaded with a 16-tap FIR interpolation filter to improve loop stability.

The PWM signal has a 4-bit time resolution, corresponding to 16 discrete pulse widths. With the frequency in the modulator loop of $256 \cdot f_s$ this results in a PWM frequency of $16 \cdot f_s$. The multi bit behavior of the PWM signal at low frequencies has a positive effect on the loop stability. Therefore, aggressive noise shaping can be used, while the modulator remains inherently stable up to high modulation depths. In this realization with a 5th order loop filter, stable behavior is guaranteed up to 85% modulation depth. A spectrum of the output of the PWM $\Sigma\Delta$ modulator with such an input is shown in . As in normal sigma-delta modulators, state limiters inside the loop filter enable 100% modulation depth, but with reduced performance, see .

Specifications

Parameter	Description	Min	Typ	Max	Units
Frequencies					
f_{CLK}	Clock frequency (input)		256		f_s
f_s	Sample frequency	0	44.1 - 48		kHz
f_{PWM}	PWM frequency		1/16		f_{CLK}
Modulator performance					
BW_{PASS}	Stopband edge for quantization noise		0.45		f_s
e_{NQ}	Inband quantization noise of the modulator		-116 -120		dBFS dBFS
DR	Dynamic range		117		dB
SNR _{MAX}	Maximum Signal to Noise Ratio		116		dB
$U_{IN,MAX}$	Maximum input without invoking limiters		-1.4		dBFS
Modulator implementation					
N_{GATES}	Number of gates / hardware cost		700		
A_{C14}	Chip area in 0.14 μ m CMOS		0.018		mm ²

Table 1: Specifications of the PWM $\Sigma\Delta$ modulator

Port list

Port name	width	Description
<i>Clk</i>	1	Clock input, at 256*fs
<i>Reset_N</i>	1	Reset input (active low), resets all states to initial condition
<i>PCM_in</i>	24	PCM input, at N*fs (as long as N*fs is synchronous to Clk)
<i>PWM_out</i>	1	PWM output

Table 2: Port function descriptions

Typical Characteristics

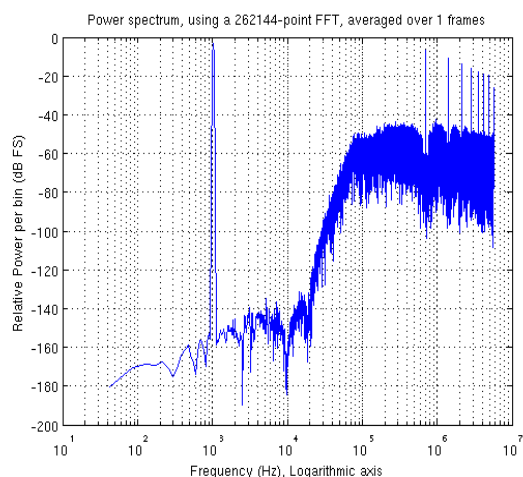


Figure 2: Output power spectrum with -1.4dBFS input and $f_s=44.1\text{kHz}$

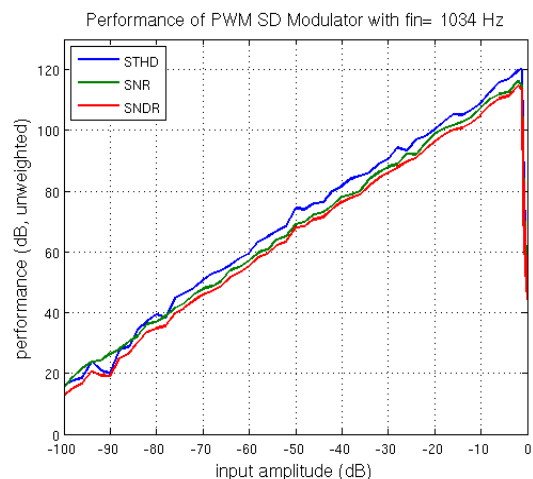


Figure 3: Modulator performance with $f_s=44.1\text{kHz}$

Deliverables

The IP deliverable consists of a RTL description in VHDL of the PWM sigma-delta modulator. The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement.

- Design unit** PWM_SD_Modulator (RTL, containing entity and architecture)
- File name** pwm_sd_modulator.vhd
- Version** 1.31F or higher
- Target** Synthesizable as ASIC logic or on FPGA
- Limitations** None known
- Errors** None known
- Dependencies**
 1. IEEE.Numeric_Std
 2. DSP_functions (package that contains general arithmetic routines, will also be delivered)

Behavioral modeling: RTL code is suitable for behavioral simulations, other types of behavioral models can be delivered upon request.

Samples: bit stream examples are available for experimentation.

References

[Door2005] T. S. Doorn, A.J.M. van Tuijl, D. Schinkel, A.J. Annema, M. Berkhout, B. Nauta, "An audio FIR-DAC in a BCD process for high power Class-D amplifiers," Proc. 31th ESSCIRC, pp. 459-462, Sept. 2005.

Revision history

Revision	Date:	Author:	Reason for revision
F1	2008-12-17	G. Hoogendijk	Initial version
F2	2009-01-08	D. Schinkel	Updated content
F3	2009-05-19	D. Schinkel	Updated deliverables

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The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement.

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