

General description

This datasheet describes a general purpose Analog to Digital Converter (ADC) for low-power applications. The converter is a charge-redistribution successive-approximation type converter.

The key feature of this ADC is its low power consumption. This is achieved by using an energy efficient comparator and by making all circuitry dynamic. As a result, quiescent current is avoided and the power consumption is fully proportional to the sample-rate. This property makes the ADC ideal for low duty-cycle sensor applications and other applications benefiting from low power consumption.

The converter can operate in both single-ended and differential mode, making it suitable for a broad range of applications.

The functional block diagram is shown in Figure 1.

The IP product described in this datasheet is silicon proven.

Features

- sample-rate up to 10 MS/s
- low power consumption, proportional to sample-rate:
740 μ W @ 10 MS/s
7.4 μ W @ 100 kS/s
- single-ended and differential mode
- 10.5 ENOB
- >80 dB SFDR (incl THD)
- 0.15 mm² in baseline 0.18 μ m CMOS
- rail-to-rail input range
- silicon proven

Applications

- low-power applications
- sensor applications
- radio baseband processing

Block diagram

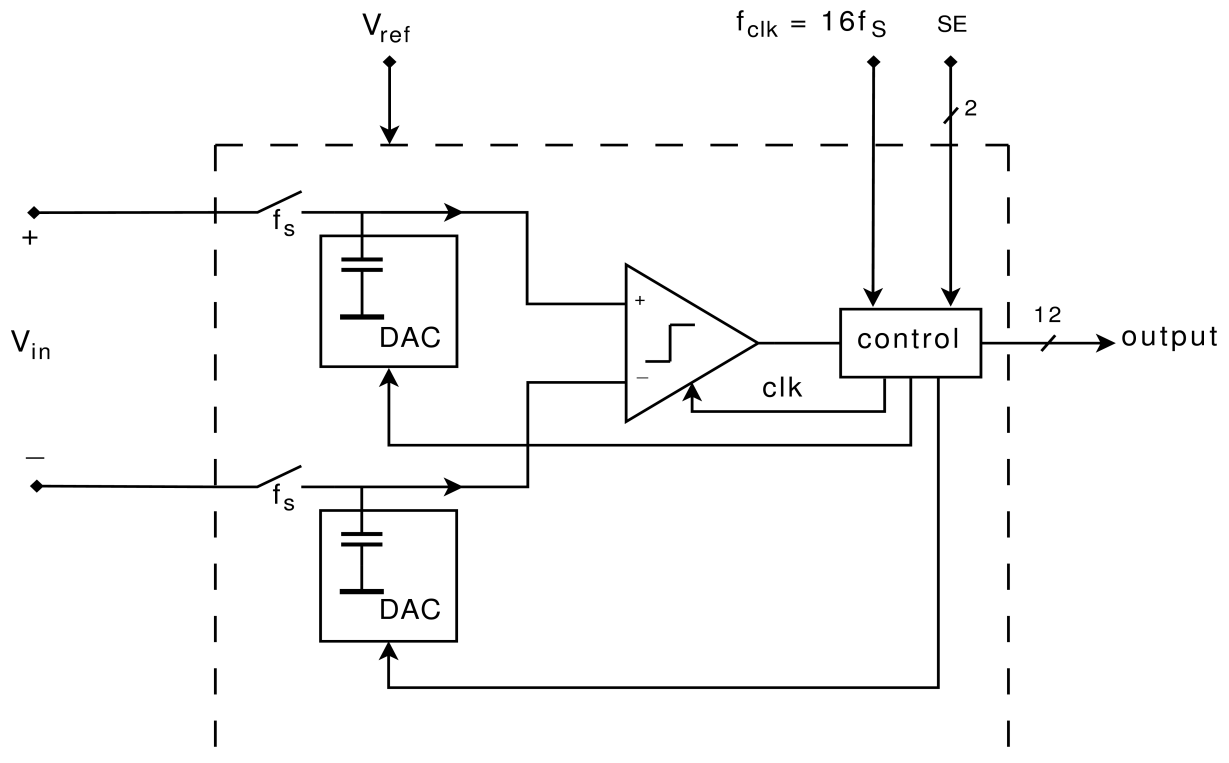


Figure 1: Block diagram of the Successive Approximation ADC.

Specifications

Default Test Conditions

Supply voltage (V_{DD})	1.8 V
Reference voltage (V_{REF})	1.0 V
Clock frequency (f_{CLK})	160 MHz (ADC sample rate: 10 MS/s)
Common-mode input voltage (V_{CM})	0.5 V
Temperature (T)	25 °C

Electrical Specifications

Parameter	Description	Min	Typ	Max	Units
Specifications					
f_s	Sample-rate	0		10	MS/s
f_{CLK}	Clock frequency (input)		16		f_s
V_{DD}	Supply voltage	1.65	1.8	1.95	V
V_{REF}	Reference voltage (without using reference buffer)	0.8	1	V_{DD}	V
V_{FS}	Full scale input voltage (single-ended)	0.98		1	V_{REF}
C_{IN}	Input capacitance (single-ended)		2		pF
I_{IN}	Input current (single-ended) (e.g. 0.7 μ A for a sample-rate of 10 MS/s)		0.07		μ A / (MS/s)
P_{ADC}	Power consumption ADC at 100 kS/s ($f_{IN} = 1.1$ kHz) 10 MS/s ($f_{IN} = 2.1$ MHz)		7.4 740		μ W
P_{BUFFER}	Reference buffer ¹⁾		790		μ W
Performance					
SFDR	Spurious Free Dynamic Range ($f_{IN} = 2.1$ MHz) (including harmonics)	80			dB
SNR	Signal to Noise Ratio ($V_{IN} = 0$ dB _{FS} , $f_{IN} = 1.1$ kHz)		66		dB
ENOB	Effective Number Of Bits ($f_{IN} = 1.1$ kHz)		10.5		bits
FoM	Figure of Merit defined as: (at both 10 MS/s and 100 kS/s)		$\frac{P}{2^{ENOB} \cdot f_s}$	0.05	pJ / conv. step
DNL	Differential Non-Linearity		± 1.5		LSB
INL	Integral Non-Linearity		± 2		LSB
Implementation					
Area	Die area in 0.18 μ m CMOS		0.15		mm ²

Table 1: Specifications of the Analog-to-Digital Converter

Notes: 1) A reference buffer is included on the test chip, which is available as a separate IP block, see section Options.

Port list

Port name	width	Description
GND	1	Ground
VDD	1	Supply voltage
VREF	1	Reference voltage, loaded with switched capacitor circuit
CLK	1	Clock signal at $16 \cdot f_s$
VIN	2	Analog input signal
SE	2	Selects which of the two inputs is used as single-ended input. If both SE signals are zero, the converter operates in differential mode.
OUT	12	Digital output signal

Table 2: Port function descriptions

Detailed description

The differential or single-ended analog input voltage (V_{IN}) in Figure 1 is sampled on the DAC capacitors with sample-rate f_s . Basically, the input impedance is purely capacitive, because at the end of the conversion, the charge on the capacitors is restored before the sample-switches are re-activated. However, due to parasitic capacitance a small DC current will flow into the input nodes. This current depends on the clock frequency.

The SE signals select which of the two inputs is used as the single-ended input; the other input should be grounded. If both SE signals are zero the converter operates in differential mode.

The ADC core requires a clock frequency (f_{CLK}) of $16 \cdot f_s$ and a buffered reference voltage (V_{REF}) that is able to drive a switched capacitor network. The capacitance of this network is around 1 pF. This buffered voltage can either be made by an on-chip reference buffer, or it can be applied externally. In case V_{DD} is sufficiently clean, it can also be used as the buffered reference voltage.

The reference voltage determines the full-scale voltage range of the ADC.

Deliverables

The IP deliverables consist of a GDS file, a behavioral model, a netlist and integration documentation. The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement.

Options

For generating the buffered reference voltage, Axiom IC offers energy-efficient reference buffers specifically aimed at this converter and adjusted to the customer's requirements.

The converter can be extended with gain and/or offset calibration.

For more information about these options, please contact us at info@axiom-ic.com.

Revision history

Revision	Date:	Reason for revision
F5	2011-02-11	Inserted missing μ -sign
F4	2010-09-17	Included description and values about input current
F3	2010-06-22	Text updates, input frequency of measurements added
F2	2010-06-16	Measurement results included, superfluous explanation removed
F1	2009-05-20	First release

Axiom IC is a design house that develops integrated circuits for silicon chips. Axiom IC focuses on the design of state-of-the-art analog and mixed signal circuits in CMOS and BiCMOS, in close cooperation with its customers. Based on our long history in industrial IC design and research, we are able to design robust ICs with short design cycles and high quality levels. Our goal is to use our expertise for customer specific design services, covering the entire range from feasibility studies and design to layout and verification.

A continuously growing IP portfolio enables us to quickly respond to customer demands giving you a short time to market. For more information please look at the web-site www.axiom-ic.com or send an e-mail to: info@axiom-ic.com

The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement.

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